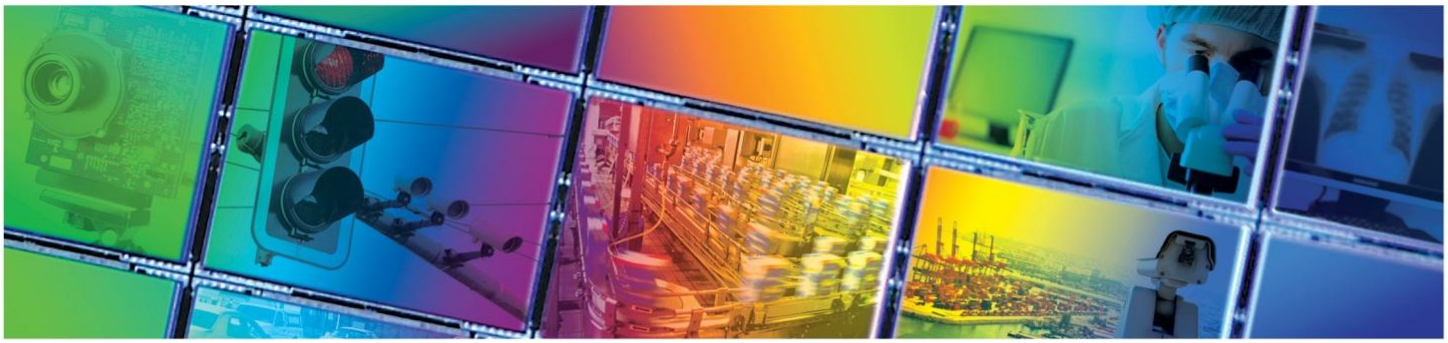
TRUESENSE imaging, inc.

KSC-1000 TIMING GENERATOR BOARD



SEPTEMBER 10, 2012

TIMING BOARD USER MANUAL

REVISION 1.0 PS-0101

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Timing Generator Board Description

This Timing Generator Board is designed to be used as part of a two-board set, used in conjunction with a Truesense Imaging CCD Imager Evaluation Board. Truesense Imaging offers a variety of CCD Imager Boards that have been designed to operate with this Timing Generator Board. For more information on the available Imager Evaluation Boards, see the Truesense Imaging contact information at the end of the document.

The Timing Generator Board generates the timing signals necessary to operate Truesense Imaging Imager Boards, and also provides the power required by these Imager Boards via the board interface connector (J6). In addition the Timing Generator Board performs the signal processing and digitization of the analog output of the Imager Board. Up to two analog outputs of the Imager Board are connected to the Timing Generator Board via coaxial cables.

The KSC-1000 Timing Generator chip provides multiple pixel-rate, line-rate, and frame rate clocks and control signals to operate Truesense Imaging CCD image sensors. The KSC-1000 is able to operate many different Interline, Full-Frame, and Linear CCD image sensors.

The Timing Generator Board contains an Altera Programmable Logic Device (PLD) that can be In-System-Programmed (ISP) with code that is imager specific. This provides flexibility to operate many different Imager Boards with the same Timing Generator Board.

The Timing Generator Board has a digital Input interface to the Altera device that can be used to support various modes of operation depending on imager-specific Altera code. The digital input interface also includes a serial interface to the KSC-1000 and AFE parts on the Timing Generator Board so that adjustments may be made to their operation, overriding the pre-programmed default operating conditions.

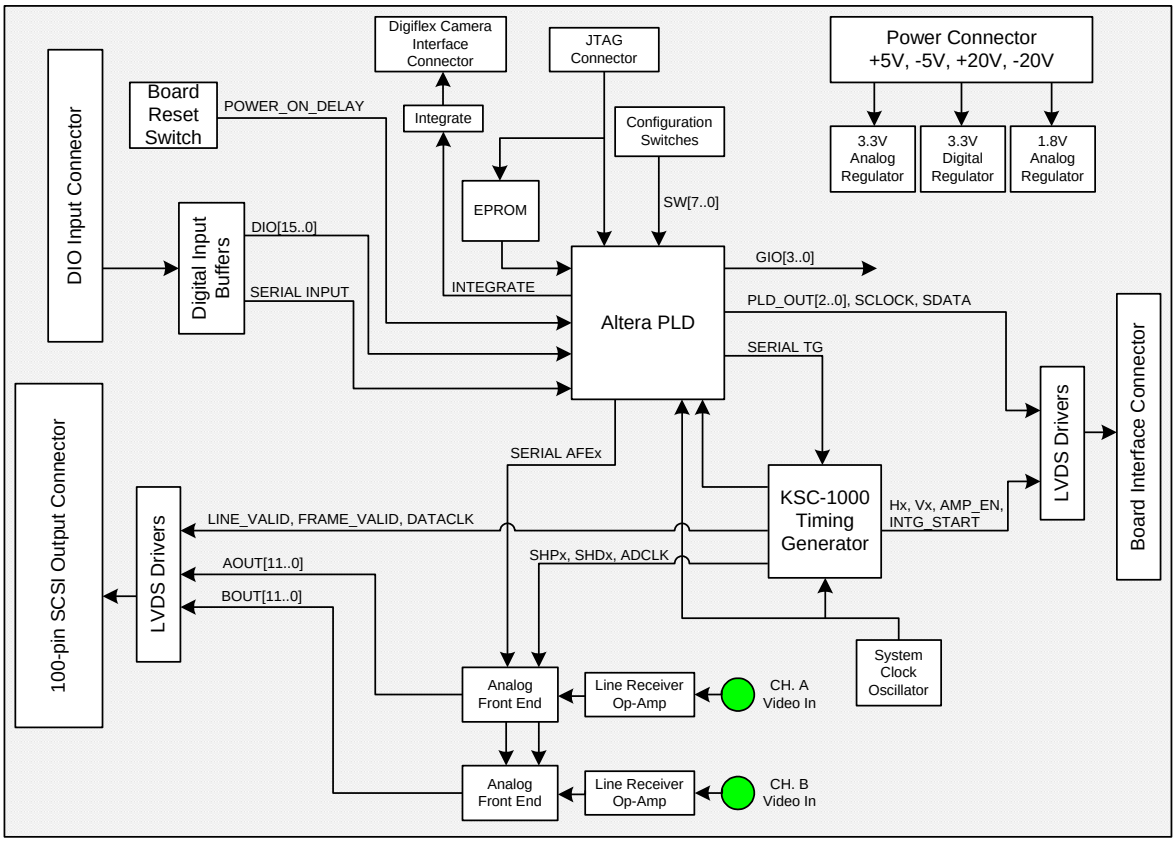

Figure 1: 3F505x/3F5579 Timing Generator Board Block Diagram

Timing Generator Board Input Requirements

The input power may be supplied by standard linear benchtop power supplies, as long as they meet the requirements of a particular Evaluation Boardset. General guidelines for these requirements are shown in Table 1; refer to the appropriate Timing Specification for the input power requirements of a particular Evaluation Boardset.

Power Supplies	Minimum	Typical	Maximum	Units
+5 V_MTR Supply	4.9	5 800	5.1	V mA
-5 V_MTR Supply	-5.1	-5 50	-4.9	V mA
VPLUS Supply	18.0	20 (Imager Board dependent)	21.0	V mA
VMINUS Supply	-18.0	-20 (Imager Board dependent)	-21.0	V mA

Table 1: Power Supply Input Requirements

Timing Generator Board Architecture Overview

The following sections describe the functional blocks of the Timing Generator Board (See Figure 1 for a block diagram).

Power Connector

The J3 power connector provides the necessary power supply inputs to the Timing Generator Board. The connector also provides the VPLUS and VMINUS power supplies. These supplies are not used by the Timing Generator Board but are needed by the CCD Imager Boards. The Timing Generator Board simply routes these power supplies from the power connector to the board interface connector.

Power Supply Filtering

Power supplied to the board is de-coupled and filtered with ferrite beads and capacitors in order to suppress noise. For best noise performance, linear power supplies should be used to provide power to the boards.

Power-On Delay / Board Reset

The POWER_ON_DELAY signal provides a reset signal to the Altera Programmable Logic Device (PLD) on power-up, or when the BOARD RESET button (S1) is pressed. The delay is generated by an RC network into a Schmitt trigger, and is approximately 400 ms, allowing power supply voltages to stabilize on the board. When the POWER_ON_DELAY signal goes high, the PLD will perform its normal power-up initialization sequence, as detailed in the applicable Timing Specification.

System Clock

The System clock is used to generate the pixel rate clocks. The pixel rate timing signals operate at a frequency that is divided down from the System clock frequency. The exact pixel rate frequency is Altera code dependent, but is limited to ½ the frequency of the System clock.

Timing Board PN	System Clock	Pixel Clock (Max)
3F5051	40 MHz	20 MHz
3F5052	56 MHz	28 MHz
3F5053	60 MHz	30 MHz
3F5054	80 MHz	40 MHz
3F5579	48 MHz	24 MHz

Table 2: Timing Board Clock Rates

Digital Input Connector

The digital input connector (J7) connects optional remote digital control signals to the evaluation board. These control signals, DIO[15..0], can be used to adjust the operating mode of the evaluation board. The function of the digital inputs depends on the Altera firmware programmed for a particular Evaluation Boardset, and is detailed in the associated Altera Code Timing Specification. This is an optional feature; no external digital inputs are required for board operation.

Any TTL-compatible digital controls may be used to control these lines. While it is recommended that these inputs range between +3.3 V (HIGH) and 0 V (LOW), voltages up to +5.0 V are acceptable.

The digital input control lines to the board are buffered. The input pins to the buffer IC's are weakly held low by pull down resistors to GND. Therefore, with no digital inputs, the default level of the control lines is all zeros.

A three-wire serial interface is also provided on the J7 input connector. The Altera PLD is programmed to decode the serial datastream, and steers the datastream to the KSC-1000 and the AFE chips as necessary. Therefore the KSC-1000 and each of the two AFE chips may be adjusted independently of one another via the serial interface, overriding the default settings stored in the Altera PLD. This is an optional feature, and is not required for board operation.

Configuration Switches

There are eight switches on the board that can be used to adjust the operating mode of the Timing Generator Board. The function of the switches depends on how the Altera device is programmed for a particular Evaluation Boardset, and is detailed in the associated Altera Code Timing Specification.

JTAG Header

This 10-pin header (J2) provides the user with the ability to reprogram the Altera PLD in place via Altera's BYTEBLASTER programming hardware.

Purchasers of a Truesense Imaging Evaluation Board Kit may, at their discretion, make changes to the Altera code firmware. Truesense Imaging Inc. can only support firmware developed and supplied by Truesense Imaging Inc. Changes to the Altera code firmware are at the risk of the customer.

When programming the Altera PLD via the JTAG interface, the Imager Board must be disconnected from the Timing Board, by removing the Board Interface Cable before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board may occur.

Integrate Output Connector

This output header (J4) provides a signal that is high during the integration time period. INTEGRATE can be used to synchronize an external shutter or LED light source with the integration time period.

The INTEGRATE signal, buffered by a transistor, is also connected to the Digiflex Camera connector (J1). This feature is optional, and the connector is not populated.

Image Sensor LVDS Drivers

Timing signals are sent to the Imager Board via the board interface connector (J6) using Low Voltage Differential Signaling (LVDS) drivers. LVDS combines high-speed connectivity with low noise and low power.

Board Interface Connector

This 80-pin connector (J6) provides both the timing signals and the necessary power to the CCD Imager Boards from the Timing Generator Board.

Altera PLD

The Programmable Logic Device (PLD) is an Altera Flex 10K series part. Paired with an EPC2 configuration EPROM, the Altera device is In System Programmable (ISP) via a 10-pin JTAG header (J2) located on the board. In this way, the Altera device is programmed with imager-specific code to operate the Imager Board to which the Timing Generator Board will be connected.

The code implemented in the Altera PLD is specific to each CCD Imager Board configuration, and is detailed in the associated Timing Specification document. At a minimum, the Altera PLD must provide these functions:

- Decode and steer serial input data to the correct device;
- Program the KSC-1000 with default settings;
- Program the AFE chips with default settings.

In addition to these functions, the Altera PLD may provide auxiliary timing and control functions for a particular CCD Imager Board. Refer to the appropriate Timing Specification for details.

Serial Input Steering

When the three-wire serial input to the Timing Board is used, the Altera PLD decodes the addressing of the serial input, and steers the datastream to the correct device. The serial input must be formatted so that the Altera PLD can correctly decode and steer the data to the correct device.

The first 3 bits in the datastream are the Device Select bits DS[2..0], sent MSB first, as shown in Figure 2. The Device Select bits are decoded as shown in Table 3.

Device Select DS[2..0]	Serial Device
000	PLD
001	AFE1
010	AFE2
011	KSC-1000
100	(Imager Board dependent)
101	(Imager Board dependent)
110	(Imager Board dependent)
111	(Imager Board dependent)

Table 3: Serial Input Device Select

The next bit in the datastream is the Read/Write bit (R/W). Only writing is supported; therefore this bit is always LOW.

The definition of next four bits in the datastream depends on the device being addressed with the Device Select bits. For the KSC-1000 device, they are Register Address bits A[3..0] LSB first. For the AD9845A or AD9840A AFE, they are Register Address bits A[2..0], LSB first, followed by a Test bit which is always set LOW.

The remaining bits in the bitstream are Data bits, LSB first, with as many bits as are required to fill the appropriate register.

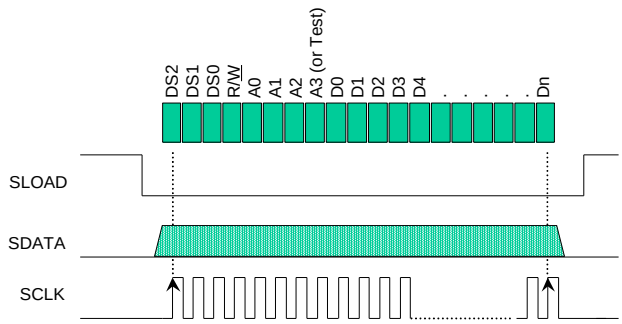

Figure 2: Serial Input Timing

The Altera PLD receives the serial datastream, decodes the Device Select address contained in the first 3 bits, and sets the appropriate SLOAD line LOW. The remaining datastream is then read in real time by the selected device. The Altera PLD does not do any checking of the datastream for correctness; it merely steers the data to the appropriate device.

KSC-1000 Default Programming

Upon power-up, or whenever the BOARD_RESET button is pressed, the Altera PLD automatically programs the registers of the KSC-1000 to their default settings via the three-wire serial interface. The default settings are specific to each CCD Imager Board configuration, and are detailed in the associated Timing Specification document.

AFE Default Programming

Upon power-up, or whenever the BOARD_RESET button is pressed, the Altera PLD automatically programs the registers of the KSC-1000 to their default settings via the three-wire serial interface. The default settings are specific to each CCD Imager Board configuration, and are detailed in the associated Timing Specification document.

Timing Board PN	Analog Devices PN	Sampling Rate	Bit Depth	Channels
3F5051	AD9845AJST	20 MSPS	12	2
3F5052	AD9845AJST	28 MSPS	12	2
3F5053	AD9845AJST	30 MSPS	12	2
3F5054	AD9840AJST	40 MSPS	10	2
3F5579	AD9845AJST	24 MSPS	12	2

Table 4: Timing Board Configuration Options

Auxiliary PLD functions

The Altera PLD may provide auxiliary timing and control functions for a particular CCD Imager Board. In addition to the Configuration switches, Remote Digital Inputs, and 3-wire Serial Interface, the inputs to the PLD include timing signals from the KSC-1000, and an auxiliary shutter control input from the (optional) J1 Digiflex Camera connector. The PLD outputs include: PLD[2..0], auxiliary outputs which are routed to the Board Interface connector (J6); HD_TG and VD_TG, timing controls signals to the KSC-1000; and ARSTZ, an asynchronous reset to the KSC-1000. These inputs and outputs allow the Altera PLD to monitor the CCD timing, and to control auxiliary functions as needed.

There are several PLD connections, GIO[2..0], that are connected only to test points (TP8, TP7, and TP6). These may be configured as PLD outputs or inputs, for extra monitoring or control.

Video Signal Processing

Each of the two signal processing channels is designed to process an analog video signal input from a CCD Imager Board. The analog video signal is buffered by an operational amplifier. This amplifier is in a non-inverting configuration with a gain of 1.25.

The output of the amplifier is then AC-coupled into the input of the AFE chip. Since the amplitude of AFE input is limited, care must be taken to adjust the gain of the Imager Board signal prior to the AFE input. The Imager Board for a particular CCD image sensor has been designed to deliver a video signal with the correct amplitude to the Timing Board, such that, when the AFE is correctly configured, optimum performance is achieved.

AD984X Analog Front End (AFE) Device

The Timing Generator Board has two analog input channels, each consisting of an operational amplifier buffer and an Analog Front End (AFE) device. The AFE chip processes the video signal, then performs the A/D conversion and outputs 10 or 12 bits of digital information per pixel. The Timing Generator Board supports the AD984X family of AFE devices offered by Analog Devices Inc.

There are several variants in the AD984X family. The Timing Generator Board is populated differently depending on which AFE device is being used. The various assembly configurations are shown in Table 4.

When using the AD9840 (10-bit, 40 MSPS) AFE, R56, R57, R63, and R64 are installed to tie what would be the least significant bits in a 12-bit system to AGND. Otherwise, these components are not installed.

The AD9840A and AD9845A AFE parts have three modes of operation with respect to the analog input signal: CCD MODE, AUX1 MODE, and AUX2 MODE. The Timing Generator Board only supports the CCD MODE. Refer to the Analog Devices AD9845A or AD9840A Specification Sheet for details.

Register Address	Register Description	Notes
0	Operation	1
1	VGA gain	1
2	Clamp	1
3	Control	1
4	PXGA 0 (CDS gain)	1,2
5	PXGA 1	1,3
6	PXGA 2	1,3
7	PXGA 3	1,3

Table 5: AFE Registers

Notes:

1. See the AD984X specifications sheet for details.
2. PXGA on the AD9845A; CDS on the AD9840A.
3. AD9845A only; not used on the AD9845A.

The AFE registers can be adjusted by re-programming the registers using the three-wire serial interface provided on the Digital Input Connector. Each AFE is independently addressable through the Altera PLD, and therefore can be adjusted independently.

Digital Image Data LVDS Drivers

Digitized image data and synchronization timing signals are sent to the computer frame-grabber hardware via the 100-pin SCSI output connector (J10) using Low Voltage Differential Signaling (LVDS) drivers. LVDS combines high-speed connectivity with low noise and low power.

SCSI Digital Output Connector

This 100-pin connector (J10) provides digitized image data and synchronization timing signals to the computer frame-grabber hardware. The output connector interfaces directly to the National Instruments PCI-1424 frame-grabber, providing two channels of 12 bit output data in parallel in LVDS differential format. The connector also provides the three necessary PCI-1424 frame-grabber synchronization signals in LVDS differential format.

KSC-1000 Timing Generator

The KSC-1000 controls the overall flow of the evaluation board operation. The TG outputs include the CCD clocks signals, AFE timing signals, and Frame Grabber synchronization signals. The KSC-1000 is configured by programming Registers, Frame Tables, and Line Tables.

Register Address	Register Description	Notes
0	Frame Table Pointer	1
1	General Setup	1
2	General Control	1
3	INTG_STRT Setup	1
4	INTG_STRT Line	1
5	Signal Polarity	1
6	Offset	1
7	Width	1
8	Frame Table Access	1
9	Line Table Access	1
10	Status	1

Table 6: KSC-1000 Registers

Notes:

1. See the KSC-1000 specification sheet for details.

Connector Assignments and Pinouts

SMB Connectors J9 and J11

J9 (Channel A) and J11 (Channel B) allow connection of analog video signal(s) from the CCD Imager Boards through correctly terminated 75 Ω coaxial cable.

Digital Input Connector J7

Pin	Assignment	Function	Pin	Assignment
1	SLOAD	SERIAL PORT	2	GND
3	SDATA	SERIAL PORT	4	GND
5	SCLOCK	SERIAL PORT	6	GND
7	DIO15	Altera Code Dependent	8	GND
9	DIO14	Altera Code Dependent	10	GND
11	DIO13	Altera Code Dependent	12	GND
13	DIO12	Altera Code Dependent	14	GND
15	DIO11	Altera Code Dependent	16	GND
17	DIO10	Altera Code Dependent	18	GND
19	DIO9	Altera Code Dependent	20	GND
21	DIO8	Altera Code Dependent	22	GND
23	DIO7	Altera Code Dependent	24	GND
25	DIO6	Altera Code Dependent	26	GND
27	DIO5	Altera Code Dependent	28	GND
29	DIO4	Altera Code Dependent	30	GND
31	DIO3	Altera Code Dependent	32	GND
33	DIO2	Altera Code Dependent	34	GND
35	DIO1	Altera Code Dependent	36	GND
37	DIO0	Altera Code Dependent	38	GND
39	NC	(not used)	40	GND

Table 7: Digital Input Connector J7

JTAG Connector J2

Pin	Assignment
1	TCK
2	AGND
3	TDO
4	+3.3 V
5	TMS
6	AGND
7	AGND
8	AGND
9	TDI
10	AGND

Table 8: JTAG Connector J2

Board Interface Connector J6

Pin	Assignment	Pin	Assignment
1	TIMING_OUT0+	2	TIMING_OUT0-
3	AGND	4	AGND
5	TIMING_OUT1+	6	TIMING_OUT1-
7	AGND	8	AGND
9	TIMING_OUT2+	10	TIMING_OUT2-
11	AGND	12	AGND
13	TIMING_OUT3+	14	TIMING_OUT3-
15	AGND	16	AGND
17	TIMING_OUT4+	18	TIMING_OUT4-
19	AGND	20	AGND
21	TIMING_OUT5+	22	TIMING_OUT5-
23	AGND	24	AGND
25	TIMING_OUT6+	26	TIMING_OUT6-
27	AGND	28	AGND
29	TIMING_OUT7+	30	TIMING_OUT7-
31	AGND	32	AGND
33	TIMING_OUT8+	34	TIMING_OUT8-
35	AGND	36	AGND
37	TIMING_OUT9+	38	TIMING_OUT9-
39	AGND	40	AGND
41	TIMING_OUT10+	42	TIMING_OUT10-
43	AGND	44	AGND
45	TIMING_OUT11+	46	TIMING_OUT11-
47	N.C.	48	N.C.
49	AGND	50	AGND
51	TIMING_OUT12+	52	TIMING_OUT12-
53	-20 V_IMG	54	-20 V_IMG
55	TIMING_OUT13+	56	TIMING_OUT13-
57	AGND	58	AGND
59	TIMING_OUT14+	60	TIMING_OUT14-
61	-5 V_MTR	62	-5 V_MTR
63	TIMING_OUT15+	64	TIMING_OUT15-
65	AGND	66	AGND
67	TIMING_OUT16+	68	TIMING_OUT16-
69	+5 V_MTR	70	+5 V_MTR
71	TIMING_OUT17+	72	TIMING_OUT17-
73	AGND	74	AGND
75	TIMING_OUT18+	76	TIMING_OUT18-
77	+20 V_IMG	78	+20 V_IMG
79	TIMING_OUT19+	80	TIMING_OUT19-

Table 9: Board Interface Connector J6

Integrate Sync Connector J4

Pin	Assignment	Function
1	INTEGRATE	signal is high during integration time period
2	AGND	GROUND

Table 10: Integrate Sync Connector J4

Power Connector J7

Pin	Assignment
1	VMINUS
2	AGND
3	VPLUS
4	AGND
5	-5 V_MTR
6	AGND
7	+5 V_MTR
8	AGND

Table 11: Power Connector J7

Configuration Switches S2 & S3

Switch	Assignment	Function
S3-1	SW0	Altera Code Dependent
S3-2	SW1	Altera Code Dependent
S3-3	SW2	Altera Code Dependent
S3-4	SW3	Altera Code Dependent
S2-1	SW4	Altera Code Dependent
S2-2	SW5	Altera Code Dependent
S2-3	SW6	Altera Code Dependent
S2-4	SW7	Altera Code Dependent

Table 12: Configuration Switches S2 & S3

Output Connector J10

Pin	Assignment	Signal Level	Pin	Assignment	Signal Level
1	AOUT0+	LVDS	2	AOUT0-	LVDS
3	AOUT1+	LVDS	4	AOUT1-	LVDS
5	AOUT2+	LVDS	6	AOUT2-	LVDS
7	AOUT3+	LVDS	8	AOUT3-	LVDS
9	AOUT4+	LVDS	10	AOUT4-	LVDS
11	AOUT5+	LVDS	12	AOUT5-	LVDS
13	AOUT6+	LVDS	14	AOUT6-	LVDS
15	AOUT7+	LVDS	16	AOUT7-	LVDS
17	AOUT8+	LVDS	18	AOUT8-	LVDS
19	AOUT9+	LVDS	20	AOUT9-	LVDS
21	AOUT10+	LVDS	22	AOUT10-	LVDS
23	AOUT11+	LVDS	24	AOUT11-	LVDS
25	N.C.		26	N.C.	
27	N.C.		28	N.C.	
29	N.C.		30	N.C.	
31	N.C.		32	N.C.	
33	N.C.		34	N.C.	
35	N.C.		36	N.C.	
37	N.C.		38	N.C.	
39	N.C.		40	N.C.	
41	FRAME+	LVDS	42	FRAME-	LVDS
43	LINE+	LVDS	44	LINE-	LVDS
45	N.C.		46	N.C.	
47	N.C.		48	N.C.	
49	PIXEL+	LVDS	50	PIXEL-	LVDS
51	BOUT0+	LVDS	52	BOUT0-	LVDS
53	BOUT1+	LVDS	54	BOUT1-	LVDS
55	BOUT2+	LVDS	56	BOUT2-	LVDS
57	BOUT3+	LVDS	58	BOUT3-	LVDS
59	BOUT4+	LVDS	60	BOUT4-	LVDS
61	BOUT5+	LVDS	62	BOUT5-	LVDS
63	BOUT6+	LVDS	64	BOUT6-	LVDS
65	BOUT7+	LVDS	66	BOUT7-	LVDS
67	BOUT8+	LVDS	68	BOUT8-	LVDS
69	BOUT9+	LVDS	70	BOUT9-	LVDS
71	BOUT10+	LVDS	72	BOUT10-	LVDS
73	BOUT11+	LVDS	74	BOUT11-	LVDS
75	N.C.		76	N.C.	
77	N.C.		78	N.C.	
79	N.C.		80	N.C.	
81	N.C.		82	N.C.	
83	N.C.		84	N.C.	
85	N.C.		86	N.C.	
87	N.C.		88	N.C.	
89	N.C.		90	N.C.	
91	N.C.		92	N.C.	
93	N.C.		94	N.C.	
95	N.C.		96	N.C.	
97	N.C.		98	N.C.	
99	AGND		100	AGND	

Table 13: Output Connector J10

Warnings and Advisories

Truesense Imaging is not responsible for customer damage to the Timing Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the Truesense Imaging Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of a Truesense Imaging Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. Truesense Imaging can only support firmware developed by, and supplied by, Truesense Imaging. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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Truesense Imaging reserves the right to change any information contained herein without notice. All information furnished by Truesense Imaging is believed to be accurate.

Revision Changes

MTD/PS-0674

Revision Number	Description of Changes
1.0	• Initial Formal Version.
2.0	• Added support for 24 MHz (3F5579) assembly. • Corrected assembly number error in Table 2 & Table 4 (3E5054 -> 3F5054).
3.0	• Updated Format and Ordering Information.

PS-0101

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template.

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