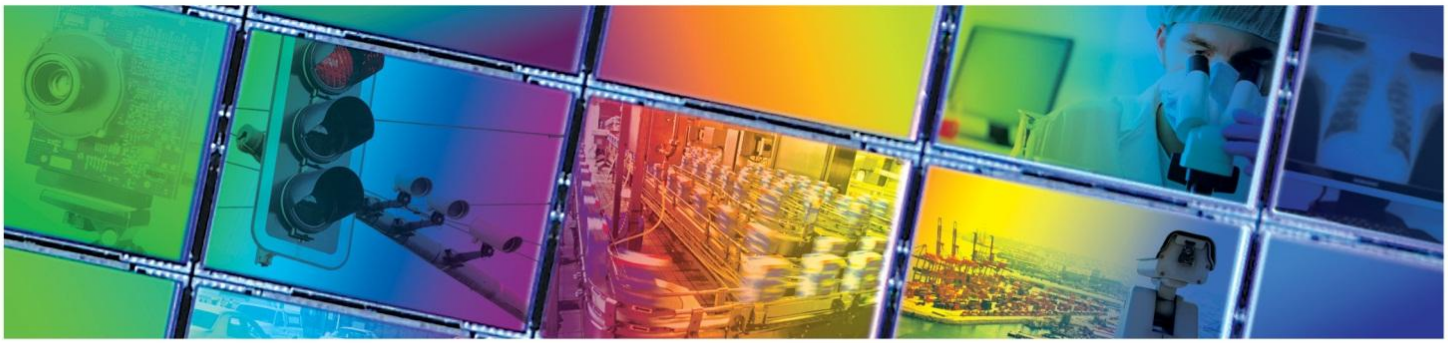
TRUESENSE imaging, inc.

VERTICAL TIMING OPTIMIZATION FOR INTERLINE CCD IMAGE SENSORS



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APPLICATION NOTE

REVISION 1.0 PS-0059

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Introduction

This application note applies to the Truesense Imaging Interline CCD Image Sensors listed in

Table 1.

On these Interline CCDs a "speed-up" structure has been incorporated to increase the frame rate. If the vertical clock pulses are not properly aligned, then these CCDs are vulnerable to a vertical striping effect. This effect is especially noticeable in a flat field image near saturation. The artifact can be eliminated by careful adjustment of the vertical clock edge alignment as described in this note.

Below is an example of vertical stripes found in the KAI-11002 Image Sensor, where there are 16 pixels between the alternating column intensities. The top portion of the image was cropped and zoomed out (50%) for illustration purposes.

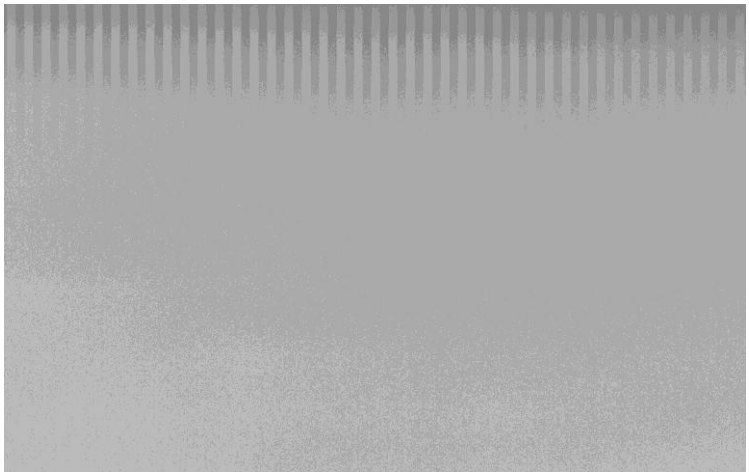

Figure 1: Example of Vertical Stripes

The spacing between stripes depends on the details of the sensor design. Please refer to the following table:

Sensor	Spacing
KAI-0340	20 pixels[1] / 10 pixels[2]
KAI-1003	16 pixels
KAI-2001	24 pixels
KAI-2020	24 pixels
KAI-2093	16 pixels
KAI-4011	8 pixels / 16 pixels
KAI-4021	8 pixels / 16 pixels
KAI-04022	8 pixels / 16 pixels
KAI-11002	16 pixels
KAI-16000	8 pixels

Table 1: Number of Pixels between Stripes

[1] Every 20 pixels for full resolution readout mode.
[2] Every 10 pixels for sub-window readout mode.

There are two cases of stripes in images:

1. Stripes run equally throughout (top-bottom) image or
2. Stripes are visible primarily in the top or bottom of image (as in Figure 1).

Depending on where the stripes appear, this will help indicate where in the timing to focus on:

For case 1, top-bottom of image, the misaligned edges are most likely in the line timing.

For case 2, top and/or bottom of image, the misaligned edges are most likely in the frame timing.

VERTICAL CLOCK EDGE ALIGNMENT SUGGESTIONS

For troubleshooting purposes, it is useful to capture flat-field images to solve this issue.

The most common solution to eliminate the vertical stripes is by trial and error adjustments to the vertical clock (V1, V2) edge positions. In general, the transition edges are desired close to coincident. A rising edge can come slightly before a falling edge, but if the opposite is true, these bars will likely appear (see Figure 2).

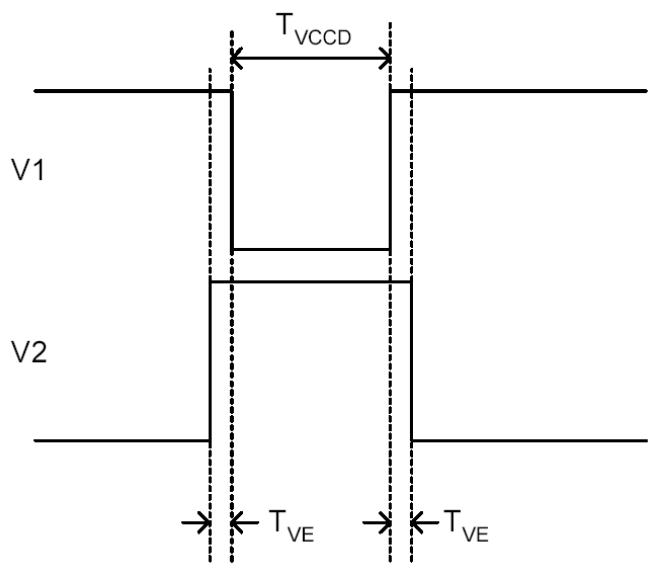

Figure 2: Example Line Timing Alignment

It is also best practice to have the clock cross points as symmetrical as possible, as shown in Figure 3 at 50% signal amplitude.

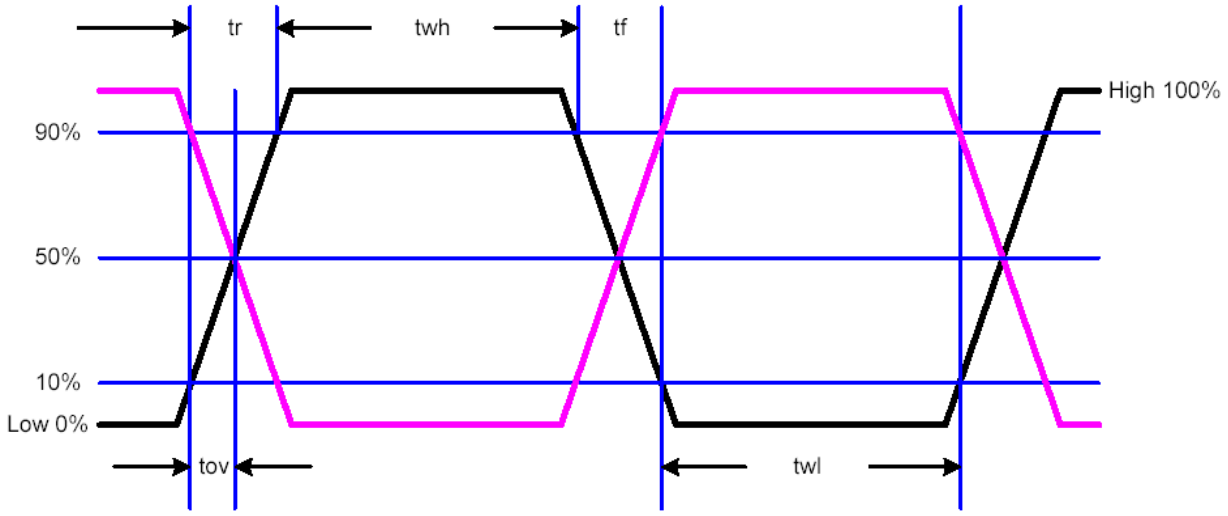

Figure 3: Symmetrical Cross points on Timing Clocks

Sometimes, a misaligned V1/V2 clock edge is accompanied by a spike on the VSUB signal. The following are suggested steps:

1. Look at V1, V2 and VSUB on an oscilloscope simultaneously.
2. Look at V1/V2 edge alignment during a row transfer, look for spikes on any of the 3 signals and adjust edge placement to eliminate.
3. Look at V1/V2 edge alignment during the frame timing (photodiode transfer) and do the same as step 2.
4. Also look at V1 and V2 where the clocks turn off and then back on for the horizontal read out. Make sure there are no glitches or spikes.
5. Look at V1, V2 and VSUB during the electronic shutter pulse and make sure there are no spikes or ringing.

Revision Changes

MTD/PS-0686

Revision Number	Description of Changes
1.0	• Initial release.
2.0	• Updated specification format.
3.0	• Updated product versions and Table 1: Number of Pixels between Stripes.

PS-0059

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template.

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