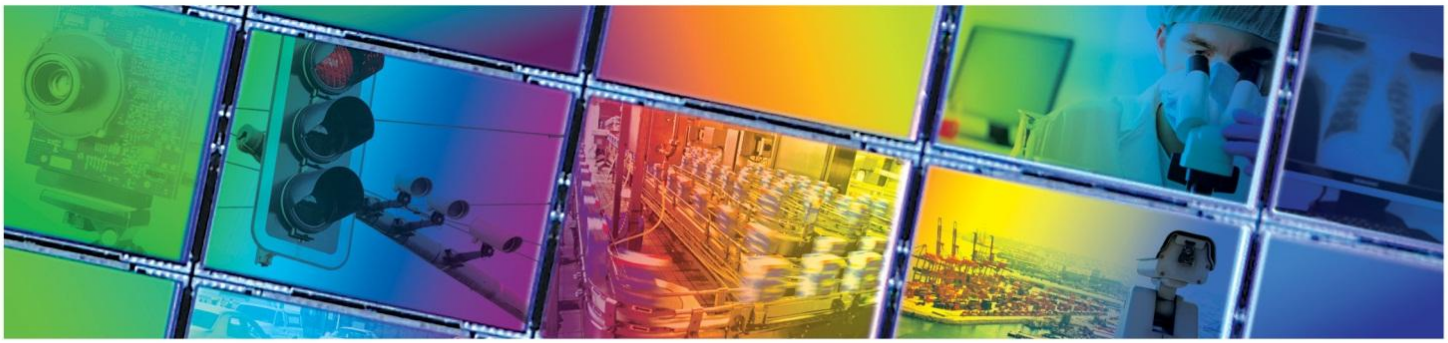
KAI-0330 IMAGER BOARD



SEPTEMBER 10, 2012

IMAGER BOARD USER MANUAL

REVISION 1.0 PS-0077

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Description

The KAI-0330 Imager Evaluation Board, referred to in this document as the Imager Board, is designed to be used as part of a two-board set, used in conjunction with a Timing Generator Board. Truesense Imaging offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KAI-0330 Image Sensors.

The Timing Generator Board generates the timing signals necessary to operate the CCD, and provides the power required by the Imager Board. The timing signals, in LVDS format, and the power, are provided to the Imager Board via the interface connector (J3). In addition, the Timing Generator Board performs the processing and digitization of the analog video output of the Imager Board.

The KAI-0330 Imager Board has been designed to operate the KAI-0330 with the specified performance at up to 30 MHz pixel clocking rate and nominal operating conditions. (See the KAI-0330 performance specification for details.)

Imager Board Input Requirements

Power Supplies	Minimum	Typical	Maximum	Units
+5 V_MTR Supply	4.9	5	5.1	V
		100		mA
-5 V_MTR Supply	-5.1	-5	-4.9	V
		50		mA
VPLUS Supply	18	20	21	V
		250		mA
VMINUS Supply	-21	-20	-18	V
		250		mA

Table 1: Power Requirements

Input Signals (LVDS)	V_{min}	$V_{threshold}$	V_{max}	Units	Comments
H1A (+/-)	0	+/- 0.1	2.4	V	H1A clock
H1B (+/-)	0	+/- 0.1	2.4	V	H1B clock
H2A (+/-)	0	+/- 0.1	2.4	V	H2 clock
H2B (+/-)	0	+/- 0.1	2.4	V	(Not Used)
R (+/-)	0	+/- 0.1	2.4	V	Reset clock
V1 (+/-)	0	+/- 0.1	2.4	V	V1 clock
V2 (+/-)	0	+/- 0.1	2.4	V	V2 clock
V3RD (+/-)	0	+/- 0.1	2.4	V	Vertical clock 3rd-level signal
VES (+/-)	0	+/- 0.1	2.4	V	Electronic Shutter signal
FDG (+/-)	0	+/- 0.1	2.4	V	Fast Dump Gate signal
V2B (+/-)	0	+/- 0.1	2.4	V	(Not Used)

Table 2: Signal Level Requirements

KAI-0330 Imager Board Architecture Overview

The following sections describe the functional blocks of the KAI-0330 Imager board (See Figure 1).

Power Filtering and Regulation

Power is supplied to the Imager Board via the J3 interface connector. The power supplies are de-coupled and filtered with ferrite beads and capacitors to suppress noise. Voltage regulators are used to create the +15 V and –15 V supplies from the VPLUS and VMINUS supplies.

LVDS Receivers / TTL Buffers

LVDS timing signals are input to the Imager Board via the J3 interface connector. These signals are shifted to TTL levels before being sent to the CCD clock drivers.

Reset Clock One-Shot

The pulse width of the RESET_CCD clock is set by a programmable One-Shot. The One-Shot can be configured to provide a RESET_CCD clock signal with a pulse width from 5 ns to 15 ns (See section Reset Clock Pulse Width).

CCD Pixel-Rate Clock Drivers (H1, H2 and Reset Clocks)

The pixel rate CCD clock drivers utilize two fast switching transistors that are designed to translate TTL-level input clock signals to the voltage levels required by the CCD. The high and low voltage levels of the CCD clocks are set by voltage dividers feeding into operational amplifiers configured as voltage followers. The current source is a high current (up to 600 mA) transistor.

CCD VCLK Drivers

The vertical clock (VCLK) drivers consist of MOSFET driver IC's. These drivers are designed to translate the TTL-level clock signals to the voltage levels required by the CCD. The high and low voltage rails of the vertical clocks are generated from the output of the positive and negative voltage regulators. The voltage level is set by a voltage divider and an operational amplifier configured as a voltage follower. The current source is a high current (up to 600 mA) transistor. The mid-level voltage is set by a voltage regulator and a diode to be several tenths of a volt above AGND. The third level of the V1_CCD clock (V3RD) is AC-coupled onto the mid-level voltage once per frame to transfer the charge from the photodiodes to the vertical CCDs.

CCD FDG Driver

The Fast Dump Gate (FDG) driver is a transistor that will switch the voltage on the FDG pin of the CCD from -5 V to +5 V during Fast Dump Gate operation. When not in operation, or when the Fast Dump Gate feature is not being utilized, the FDG pin of the CCD is held at -5 V.

VES Circuit

The quiescent CCD substrate voltage (VSUB) is set via a potentiometer. For electronic shutter operation, the VES signal drives a transistor amplifier which AC-couples the voltage difference between the VPLUS and VMINUS supplies onto the Substrate voltage. This creates the necessary potential to clear all charge from the photodiodes, thereby acting as an electronic shutter to control exposure.

CCD Bias Voltages

The bias voltages are set by voltage dividers. The bias voltages are de-coupled at the CCD pin.

CCD Image Sensor

This evaluation board supports the KAI-0330 Image Sensor.

Emitter-Followers

The VOUT_CCD signals are buffered using a bipolar junction transistor in the emitter-follower configuration. This circuit also provides the necessary current sink for the CCD output circuit.

Line Drivers

The buffered VOUT_CCD signals are AC-coupled and driven from the Imager Board by operational amplifiers in a non-inverting configuration. The operational amplifiers are configured to have a gain of 2, to correctly drive 75 Ω video coaxial cabling from the SMB connectors (see SMB Connectors J1 AND J2).

KAI-0330 Operational Settings

The Imager board is configured to operate the KAI-0330 under the following operating conditions:

Bias Voltages

Description	Symbol	Setting	Units	Notes
Output Amplifier Supply	VDD	15	V	
Reset Drain	VRD	9	V	
Output Amplifier Return	VSS	0	V	
Ground, P-Well	GND	0	V	
Substrate	VSUB	10	V	VSUB is adjustable via R56
Fast Dump Gate	FDG	-5	V	Held at –5 V when the FDG Option disabled
P-WELL	WELL	0	V	

Table 3: Bias Voltages

Clock Voltages

Description	Symbol	Low	Mid	High	Units	Notes
Phase 1 Horizontal Clock	H1A_CCD	-7	-	3	V	
Phase 1 Horizontal Clock	H1B_CCD	-7	-	3	V	
Phase 2 Horizontal Clock	H2_CCD	-7	-	3	V	
Phase 1 Vertical Clock	V1_CCD	-9.5	0.2	9	V	
Phase 2 Vertical Clock	V2_CCD	-9.5	0.2	9	V	
Reset Clock	RESET_CCD	-6	-	0	V	R- is adjustable via R28
Fast Dump Gate Clock	FDG_CCD	-5	-	5	V	

Table 4: Clock Voltages

Reset Clock Pulse Width

The pulse width of RESET_CCD is set by configuring P[2..0], the inputs to the programmable one-shot. P[2..0] can be tied high or low to achieve the desired pulse width by populating the resistors R33-38 accordingly.

Pulse Width	P0	P1	P2	R33	R34	R35	R36	R37	R38	Notes
15 ns	0	0	0	OUT	OUT	OUT	IN	IN	IN	
5 ns	1	0	0	OUT	OUT	IN	IN	IN	OUT	(Default Setting)
7.5 ns	0	1	0	OUT	IN	OUT	IN	OUT	IN	
10 ns	1	1	0	OUT	IN	IN	IN	OUT	OUT	
12.5 ns	0	0	1	IN	OUT	OUT	OUT	IN	IN	
15 ns	1	0	1	IN	OUT	IN	OUT	IN	OUT	
15 ns	0	1	1	IN	IN	OUT	OUT	OUT	IN	
15 ns	1	1	1	IN	IN	IN	OUT	OUT	OUT	

Table 5: Reset Clock Pulse Width

Block Diagram and Performance Data

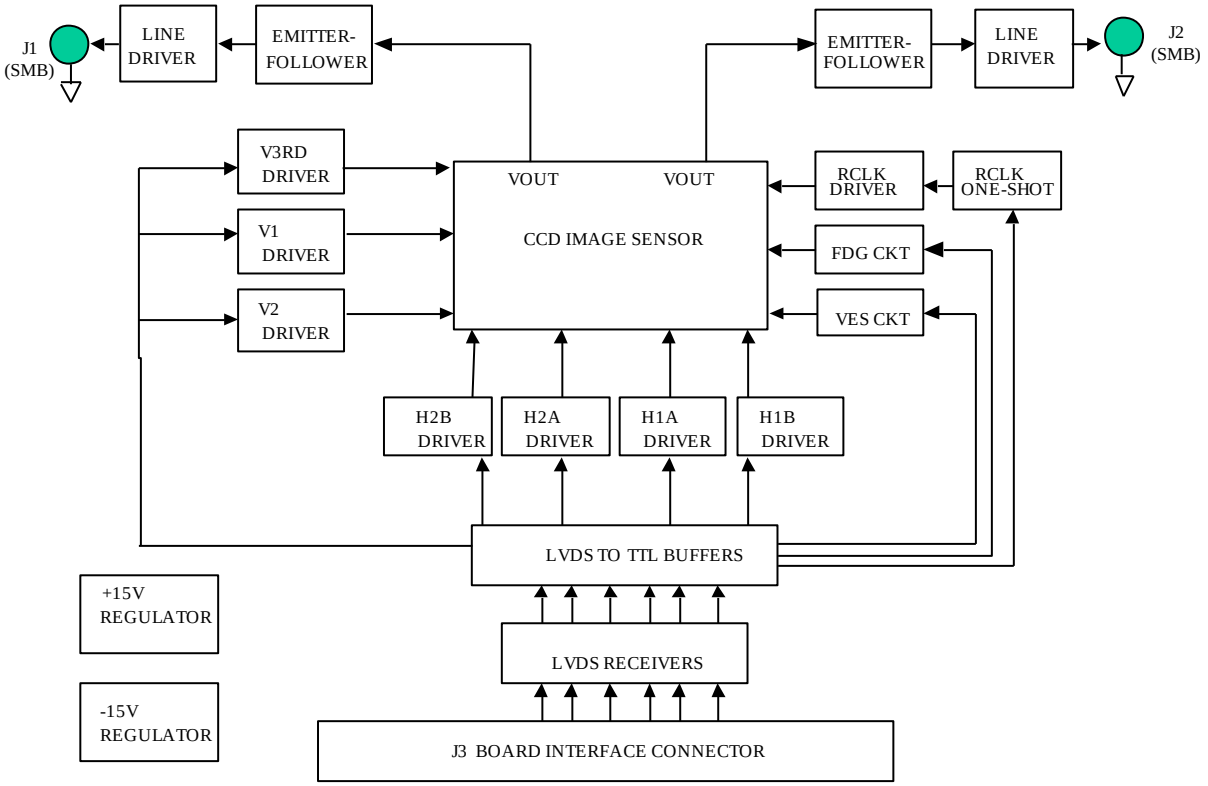

Figure 1: KAI-0330 Imager Board Block Diagram

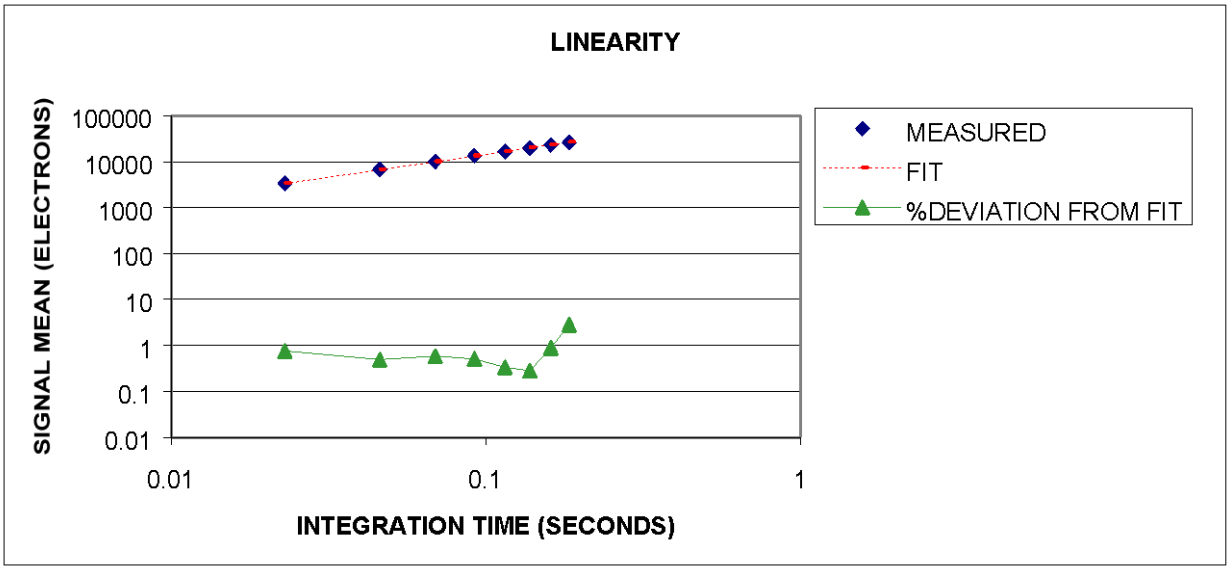

Figure 2: Measured Performance @ 20 MHz – Linearity

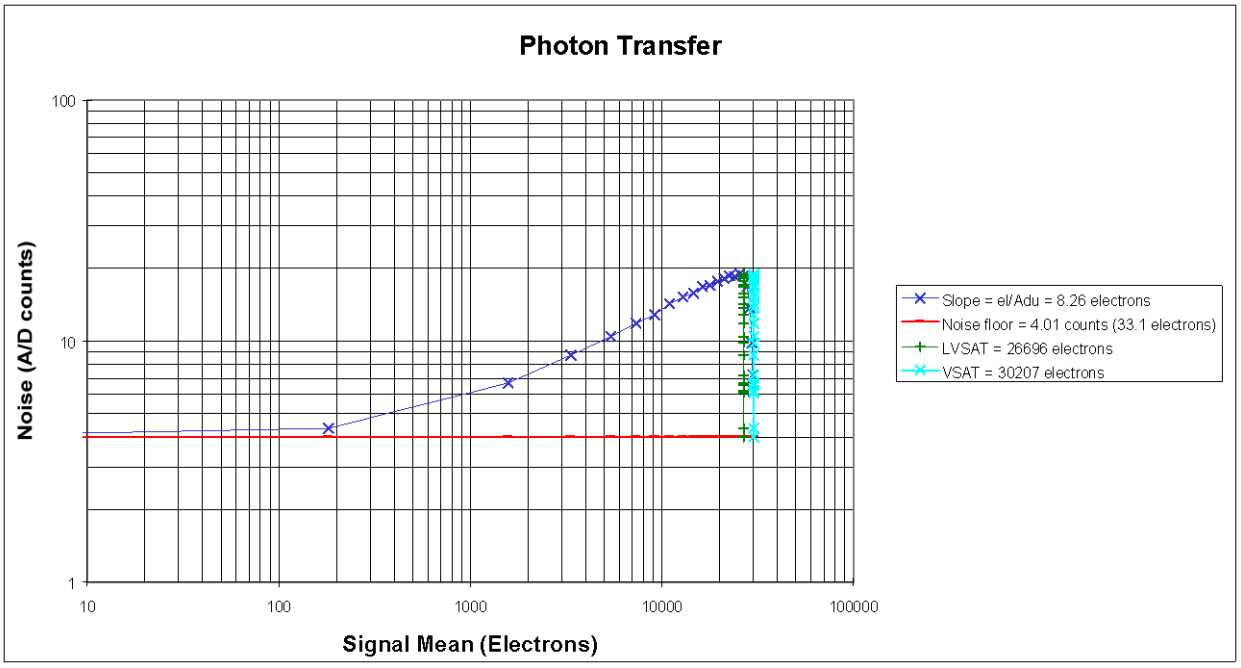

Figure 3: Measured Performance @ 20 MHz - Dynamic Range and Noise Floor

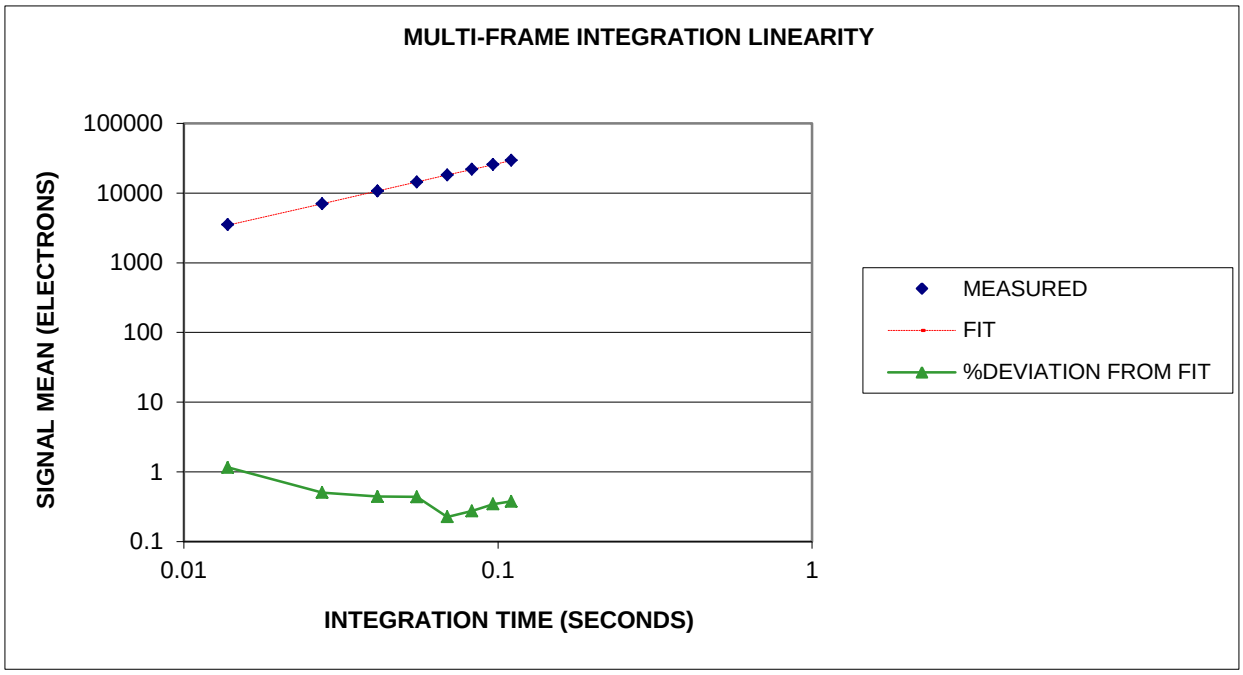

Figure 4: Measured Performance @ 30 MHz – Linearity

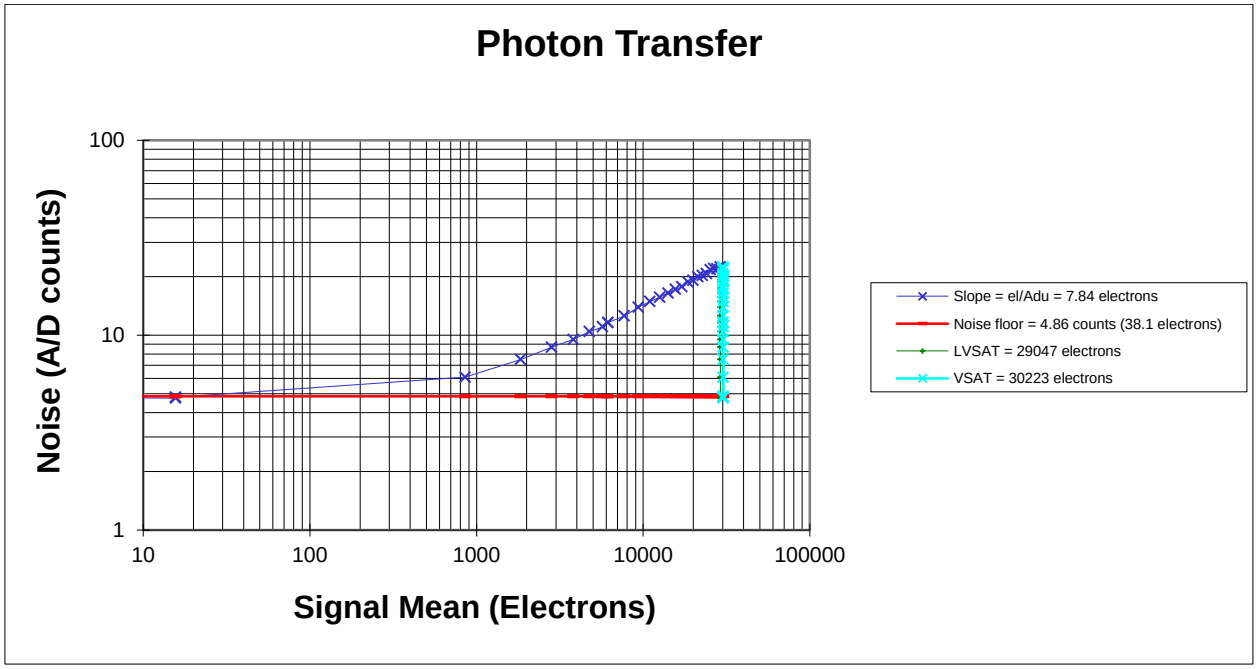

Figure 5: Measured Performance @ 30 MHz -- Dynamic Range and Noise Floor

Connector Assignments and Pinouts

SMB Connectors J1 AND J2

The emitter-follower buffered CCD_VOUT signals are driven from the Imager Board via the SMB connector J1 and J2. Coaxial cable with a characteristic impedance of 75 Ω should be used to connect the imager board to the Timing Generator Board to match the series and terminating resistors used on these boards.

Board Interface Connector J3

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	AGND	4	AGND
5	VES+	6	VES-
7	AGND	8	AGND
9	FDG+	10	FDG-
11	AGND	12	AGND
13	V3RD+	14	V3RD-
15	AGND	16	AGND
17	V2B+	18	V2B-
19	AGND	20	AGND
21	V2+	22	V2-
23	AGND	24	AGND
25	V1+	26	V1-
27	AGND	28	AGND
29	R+	30	R-
31	AGND	32	AGND
33	H2B+	34	H2B-
35	AGND	36	AGND
37	H2A+	38	H2A-
39	AGND	40	AGND
41	H1B+	42	H1B-
43	AGND	44	AGND
45	H1A+	46	H1A-
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	N.C.	60	N.C.
61	-5 V_MTR	62	-5 V_MTR
63	N.C.	64	N.C.
65	AGND	66	AGND
67	N.C.	68	N.C.
69	+5 V_MTR	70	+5 V_MTR
71	N.C.	72	N.C.
73	AGND	74	AGND
75	N.C.	76	N.C.
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

Table 6: J3 Interface Connector Pin Assignments

Warnings and Advisories

Truesense Imaging is not responsible for customer damage to the Imager Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the Truesense Imaging Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of a Truesense Imaging Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. Truesense Imaging can only support firmware developed by, and supplied by, Truesense Imaging. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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Revision Changes

MTD/PS-0340

Revision Number	Description of Changes
1.0	• Initial Formal Version.
2.0	• Updated Format.

PS-0077

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template.

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